

FIG. 1

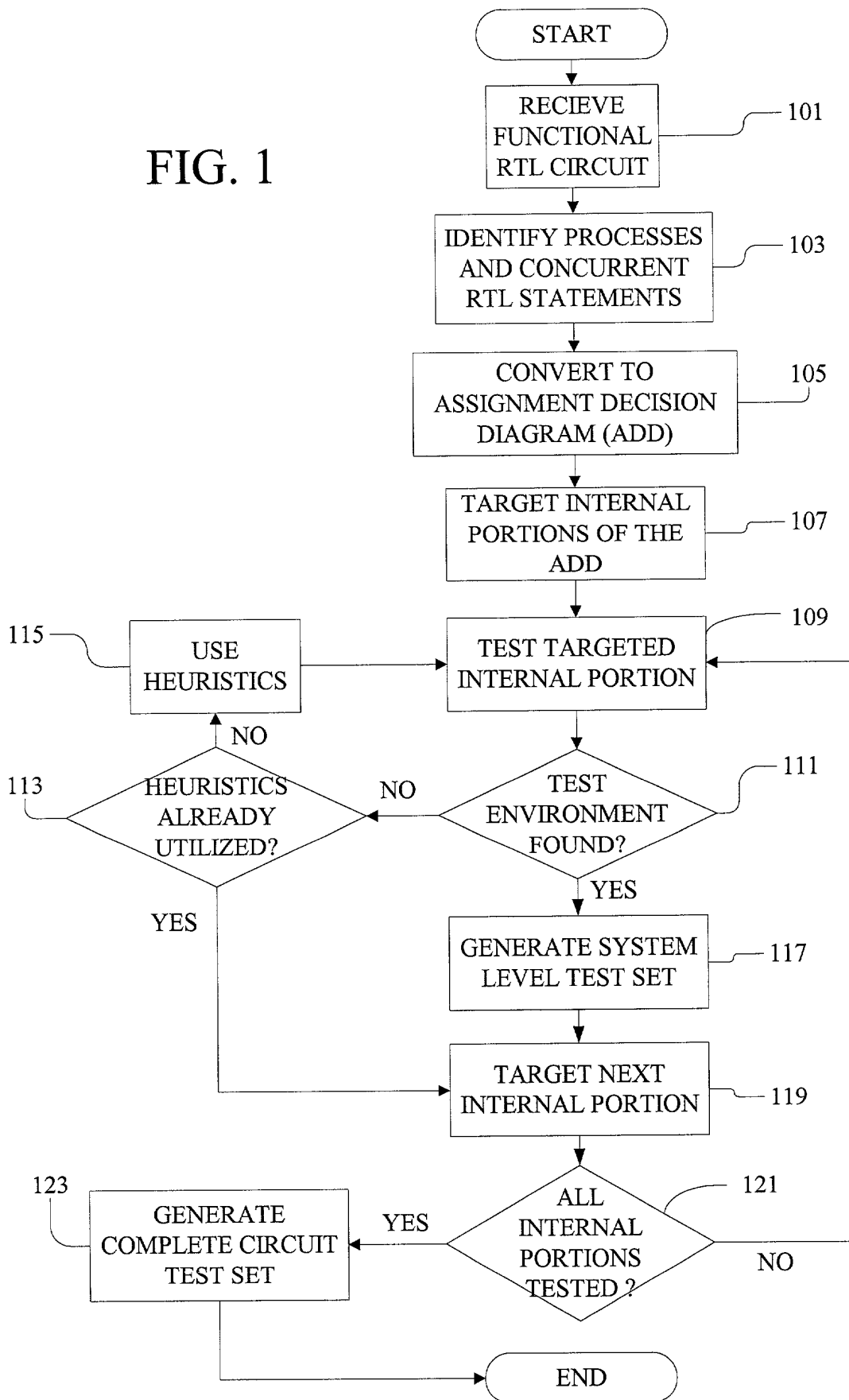


FIG. 2 is a block diagram of a logic circuit 20. The circuit 20 includes a first logic block 23, a second logic block 25, and a third logic block 27. The first logic block 23 includes registers R3, R4, R5, and R6. Register R3 contains the value 'a', register R4 contains the value '7', register R5 is a STATE REGISTER, and register R6 contains the value 'ST0'. The first logic block 23 also includes logic elements: a less-than operator (<) receiving inputs from R3 and R4, an equals operator (=) receiving inputs from R5 and R6, a NOT operator (!) receiving input from the less-than operator, an AND operator (&) receiving inputs from the less-than operator and the equals operator, and another AND operator (&) receiving inputs from the NOT operator and the first AND operator. The output of the first AND operator is labeled O6, and the output of the second AND operator is labeled O7. The second logic block 25 includes registers R1 and R2, logic elements: a subtraction operator (-) receiving inputs from R1 and R2, and an addition operator (+) receiving inputs from R1 and R2. The output of the subtraction operator is labeled O1, and the output of the addition operator is labeled O2. The third logic block 27 includes a multiplexer ADN1 receiving inputs from O1 and O2, and a register R receiving input from the multiplexer. The output of the multiplexer is labeled WI1. The circuit 20 also includes control signals: AI1 and AI2, which are inputs to the multiplexer ADN1, and AS1 and AS2, which are inputs to the second AND operator in the first logic block 23. The circuit 20 is controlled by a signal 21, which is an input to the multiplexer ADN1, and a signal 25, which is an input to the second AND operator in the first logic block 23. The circuit 20 is also controlled by a signal 27, which is an input to the register R in the third logic block 27.

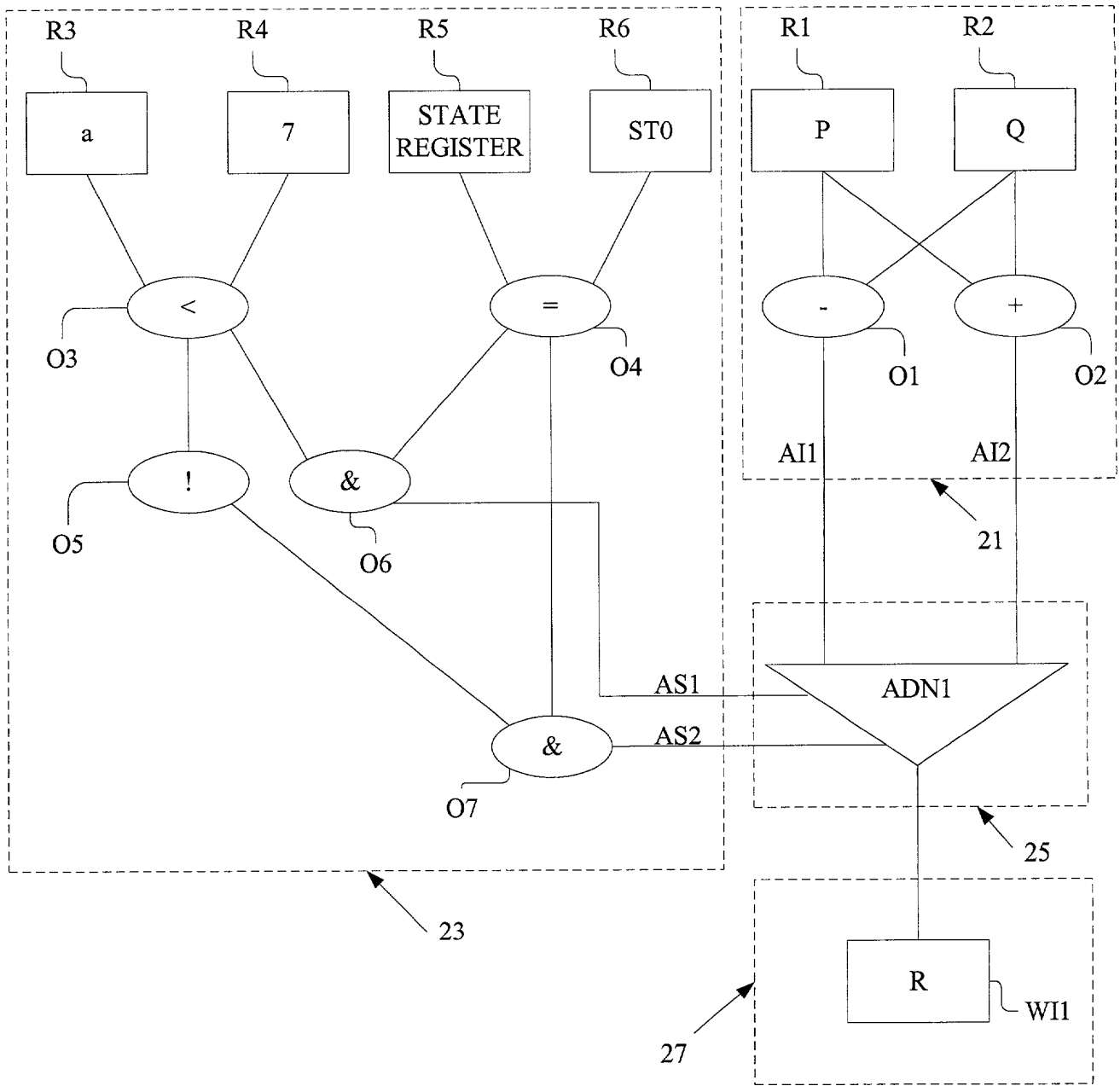


FIG. 2

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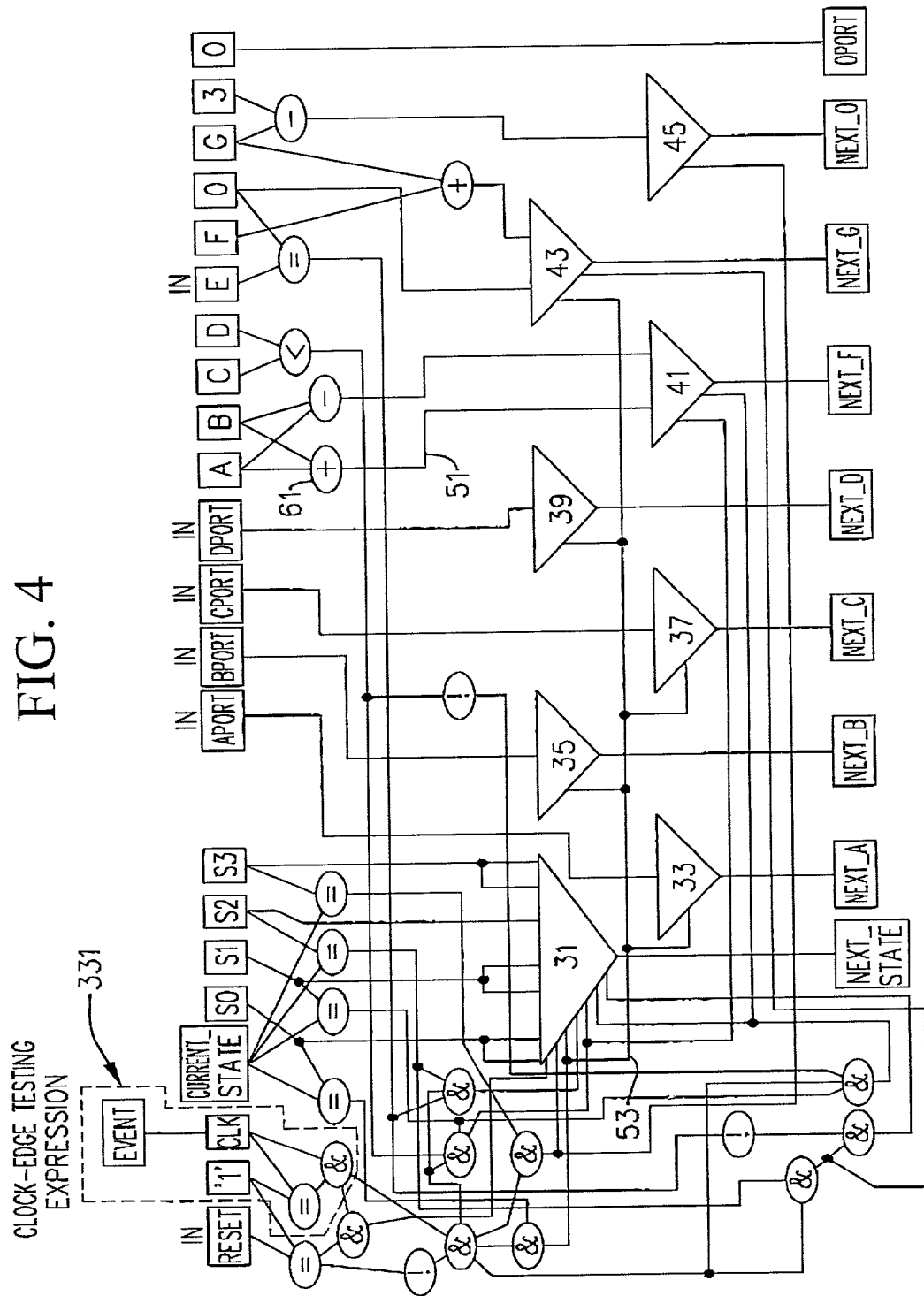
entity T1 is
  port ( RESET, CLK :IN std_logic;
        APORT, BPORT, CPORT, DPORT : IN std_logic_vector (7 downto 0);
        E : IN std_logic;
        OPORT : OUT std_logic_vector (7 downto 0) );
  end T1;
architecture RTL of T1 is
  type STATE_TYPE is ( S0, S1, S2, S3);
  signal CURRENT_STATE, NEXT_STATE : STATE_TYPE;
  SIGNAL A, B, C, D, F, G, O, NEXT_A, NEXT_B, NEXT_C, NEXT_D,
        NEXT_F, NEXT_G, NEXT_O : std_logic_vector (7 downto 0);

  begin
    COMBIN : process (CURRENT_STATE)
      begin
        NEXT_A <= A; NEXT_B <= B; NEXT_C <= C; NEXT_D <= D;
        NEXT_F <= F; NEXT_G <= G; NEXT_O <= O; OPORT <= O;
        case CURRENT_STATE is
          when S0 =>
            NEXT_A <= APORT; NEXT_B <= BPORT;
            NEXT_C <= CPORT; NEXT_D <= D;
            NEXT_G <= "00000000";
          when S1 =>
            if ( C < D ) then
              NEXT_F <= A + B;
              NEXT_STATE <= S2;
            else
              NEXT_F <= A - B;
              NEXT_STATE <= S3;
            end if;
          when S2 =>
            NEXT_G <= F + G;
            if ( E = '0' ) then
              NEXT_STATE <= S1;
            else
              NEXT_STATE <= S3;
            end if;
          when S3 =>
            NEXT_O <= G - 3;
            NEXT_STATE <= S0;
          end case;
        end process;

    SYNCH : process (CLK, RESET)
      begin
        if ( CLK'event and CLK = '1' ) then
          if ( RESET = '1' ) then
            CURRENT_STATE <= S0;
          else
            A <= NEXT_A; B <= NEXT_B; C <= NEXT_C; D <= NEXT_D;
            G <= NEXT_G; F <= NEXT_F; O <= NEXT_O;
          end if;
        end if;
      end process;
    end RTL;
  
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FIG. 3

FIG. 4



41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100 101 102 103 104 105 106 107 108 109 110 111 112 113 114 115 116 117 118 119 120 121 122 123 124 125 126 127 128 129 130 131 132 133 134 135 136 137 138 139 140 141 142 143 144 145 146 147 148 149 150 151 152 153 154 155 156 157 158 159 160 161 162 163 164 165 166 167 168 169 170 171 172 173 174 175 176 177 178 179 180 181 182 183 184 185 186 187 188 189 190 191 192 193 194 195 196 197 198 199 200 201 202 203 204 205 206 207 208 209 210 211 212 213 214 215 216 217 218 219 220 221 222 223 224 225 226 227 228 229 230 231 232 233 234 235 236 237 238 239 240 241 242 243 244 245 246 247 248 249 250 251 252 253 254 255 256 257 258 259 260 261 262 263 264 265 266 267 268 269 270 271 272 273 274 275 276 277 278 279 280 281 282 283 284 285 286 287 288 289 290 291 292 293 294 295 296 297 298 299 300 301 302 303 304 305 306 307 308 309 310 311 312 313 314 315 316 317 318 319 320 321 322 323 324 325 326 327 328 329 330 331 332 333 334 335 336 337 338 339 340 341 342 343 344 345 346 347 348 349 350 351 352 353 354 355 356 357 358 359 360 361 362 363 364 365 366 367 368 369 370 371 372 373 374 375 376 377 378 379 380 381 382 383 384 385 386 387 388 389 390 391 392 393 394 395 396 397 398 399 400 401 402 403 404 405 406 407 408 409 410 411 412 413 414 415 416 417 418 419 420 421 422 423 424 425 426 427 428 429 430 431 432 433 434 435 436 437 438 439 440 441 442 443 444 445 446 447 448 449 450 451 452 453 454 455 456 457 458 459 460 461 462 463 464 465 466 467 468 469 470 471 472 473 474 475 476 477 478 479 480 481 482 483 484 485 486 487 488 489 490 491 492 493 494 495 496 497 498 499 500 501 502 503 504 505 506 507 508 509 510 511 512 513 514 515 516 517 518 519 520 521 522 523 524 525 526 527 528 529 530 531 532 533 534 535 536 537 538 539 540 541 542 543 544 545 546 547 548 549 550 551 552 553 554 555 556 557 558 559 560 561 562 563 564 565 566 567 568 569 570 571 572 573 574 575 576 577 578 579 580 581 582 583 584 585 586 587 588 589 590 591 592 593 594 595 596 597 598 599 600 601 602 603 604 605 606 607 608 609 610 611 612 613 614 615 616 617 618 619 620 621 622 623 624 625 626 627 628 629 630 631 632 633 634 635 636 637 638 639 640 641 642 643 644 645 646 647 648 649 650 651 652 653 654 655 656 657 658 659 660 661 662 663 664 665 666 667 668 669 670 671 672 673 674 675 676 677 678 679 680 681 682 683 684 685 686 687 688 689 690 691 692 693 694 695 696 697 698 699 700 701 702 703 704 705 706 707 708 709 710 711 712 713 714 715 716 717 718 719 720 721 722 723 724 725 726 727 728 729 730 731 732 733 734 735 736 737 738 739 740 741 742 743 744 745 746 747 748 749 750 751 752 753 754 755 756 757 758 759 760 761 762 763 764 765 766 767 768 769 770 771 772 773 774 775 776 777 778 779 780 781 782 783 784 785 786 787 788 789 790 791 792 793 794 795 796 797 798 799 800 801 802 803 804 805 806 807 808 809 810 811 812 813 814 815 816 817 818 819 820 821 822 823 824 825 826 827 828 829 830 831 832 833 834 835 836 837 838 839 840 841 842 843 844 845 846 847 848 849 850 851 852 853 854 855 856 857 858 859 860 861 862 863 864 865 866 867 868 869 870 871 872 873 874 875 876 877 878 879 880 881 882 883 884 885 886 887 888 889 890 891 892 893 894 895 896 897 898 899 900 901 902 903 904 905 906 907 908 909 910 911 912 913 914 915 916 917 918 919 920 921 922 923 924 925 926 927 928 929 930 931 932 933 934 935 936 937 938 939 940 941 942 943 944 945 946 947 948 949 950 951 952 953 954 955 956 957 958 959 960 961 962 963 964 965 966 967 968 969 970 971 972 973 974 975 976 977 978 979 980 981 982 983 984 985 986 987 988 989 990 991 992 993 994 995 996 997 998 999 1000

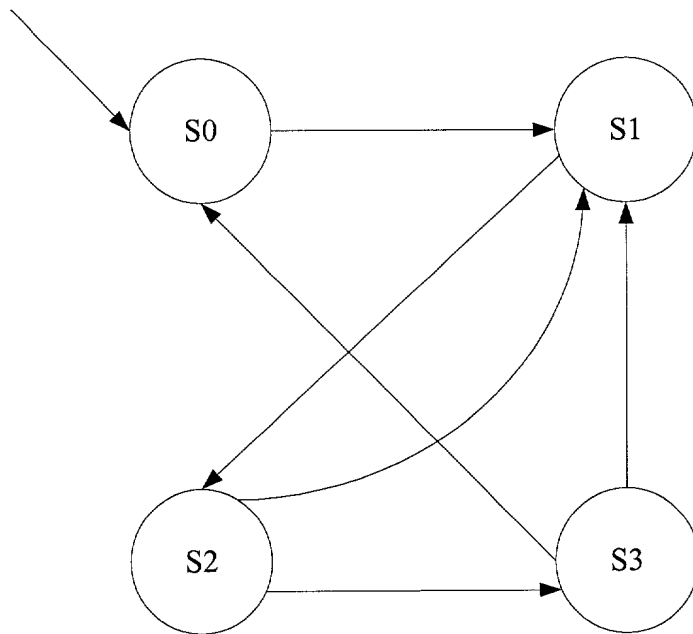


FIG. 5

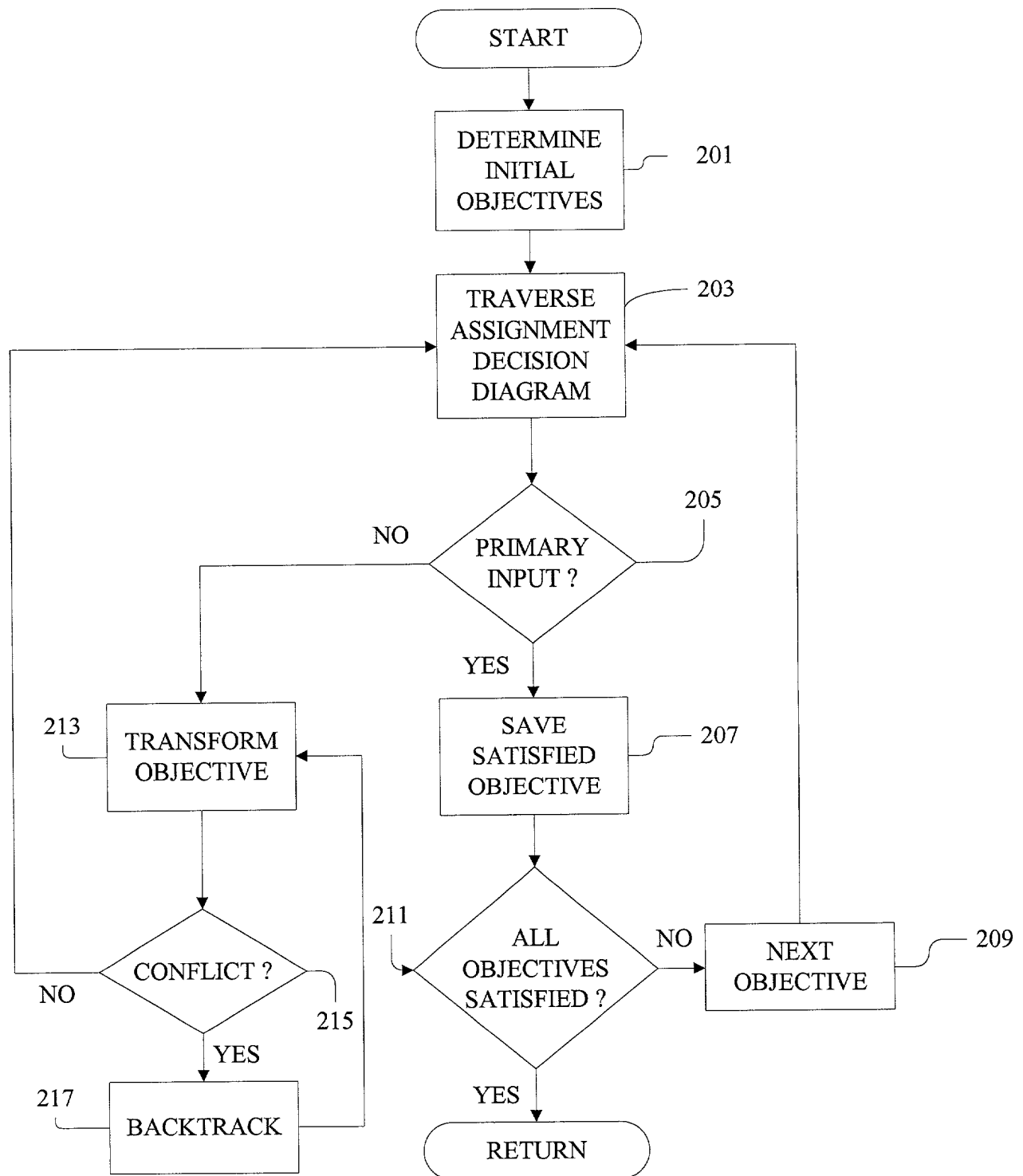


FIG. 6

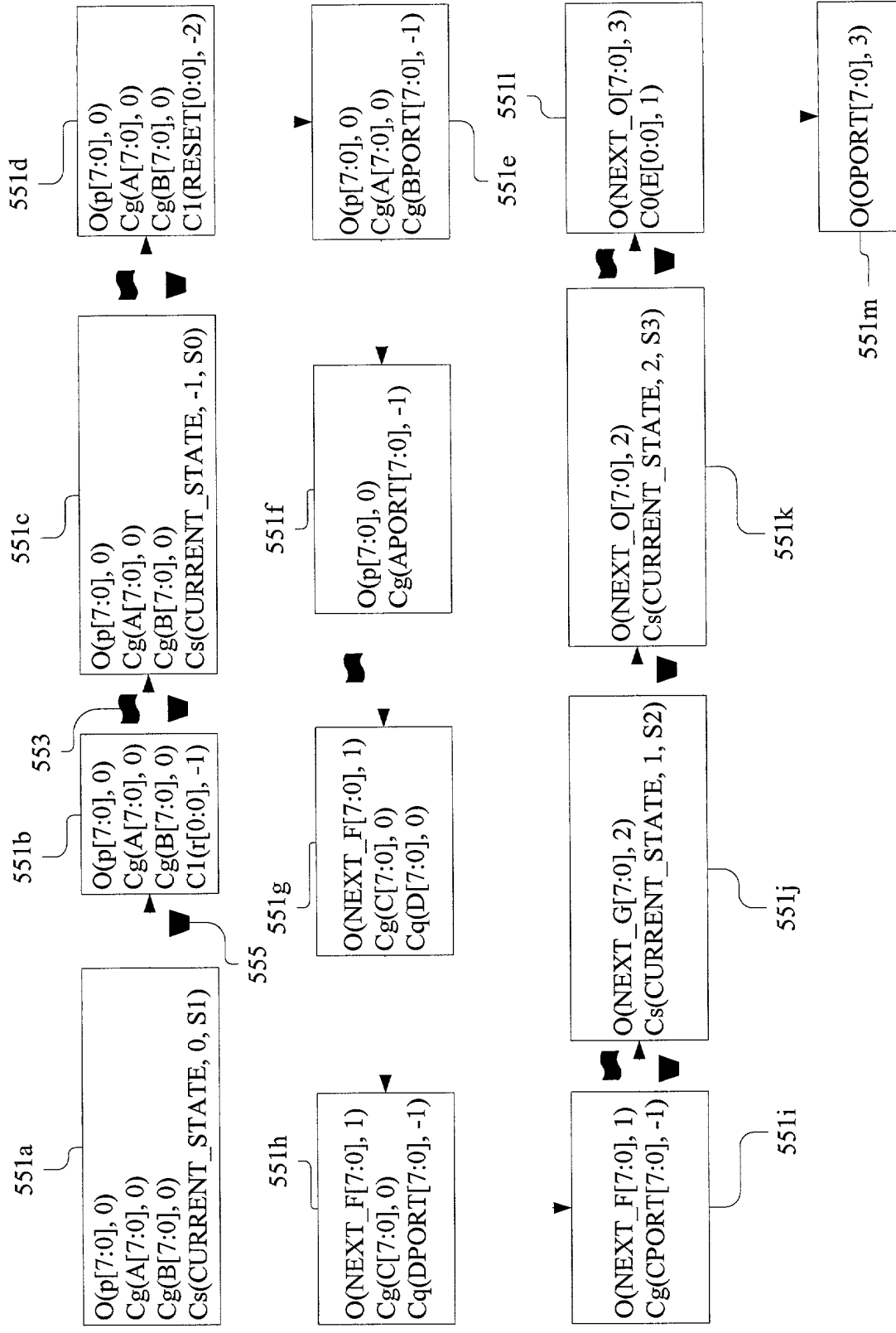


FIG. 7

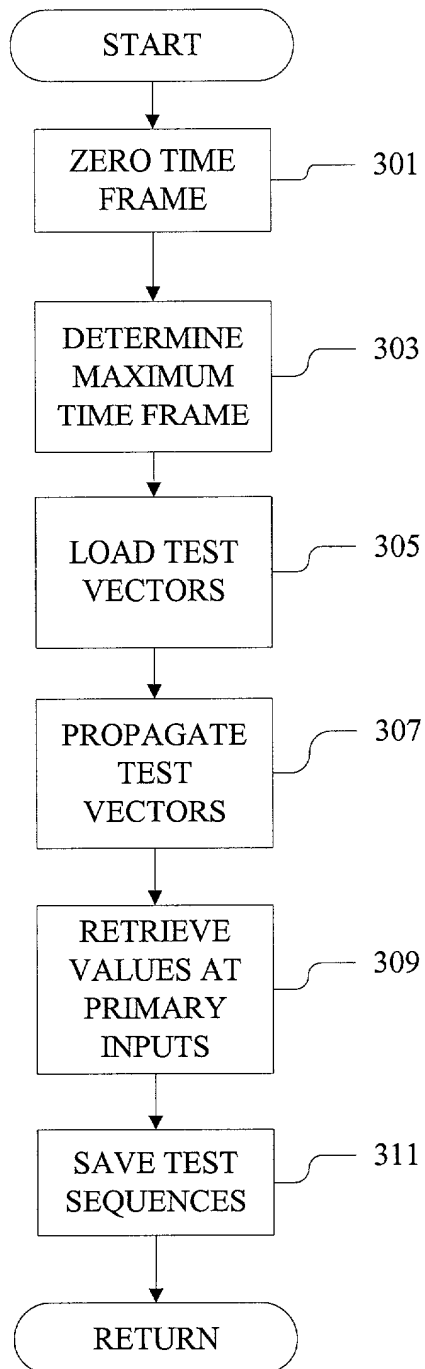


FIG. 8

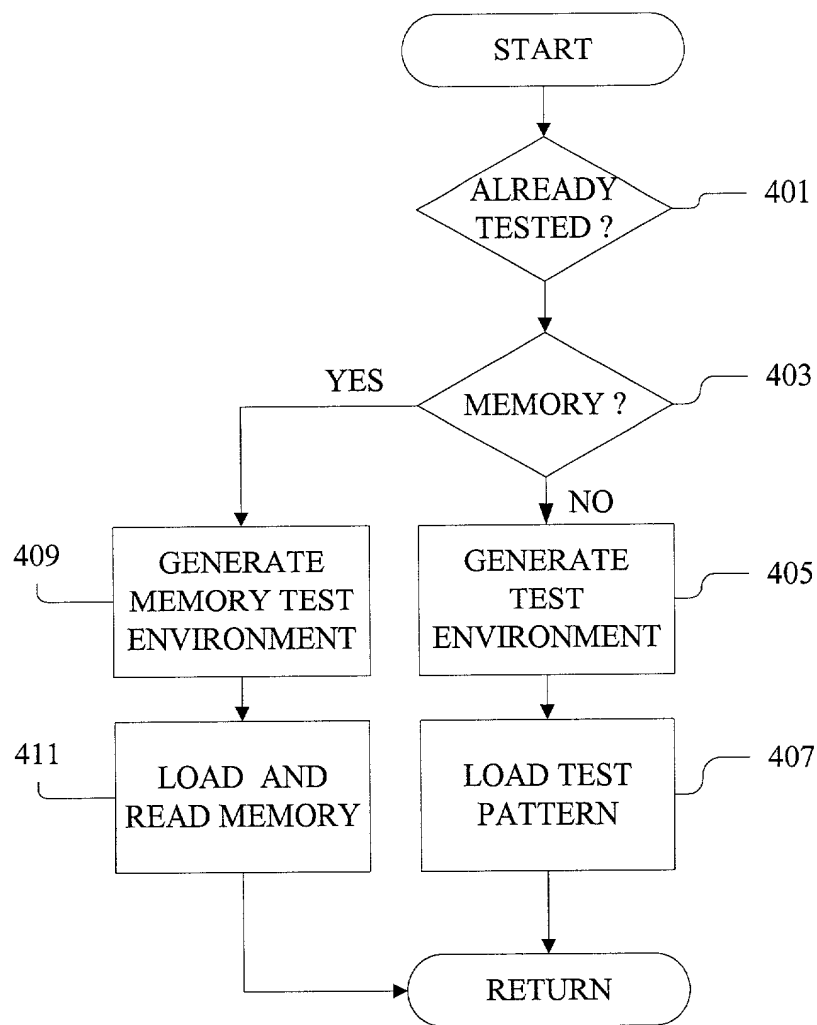


FIG. 9

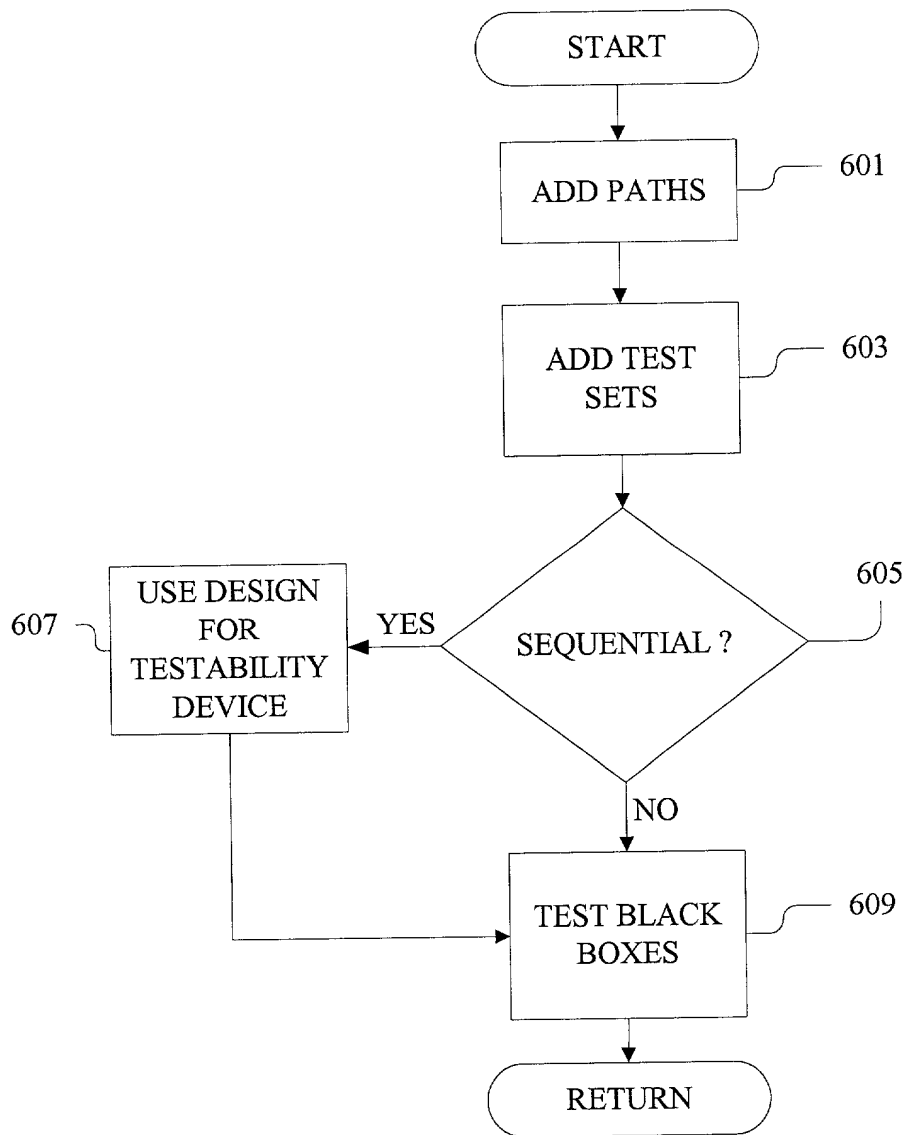


FIG. 10